each frame will have to be tampered with which is difficult to do so. Thus, this aspect of the present invention gives greater veracity of data.

If it can be seen that the ability to compress the data means that a smaller communications band-width can be used, and it is easier to provide data buffers to cope with the information.

The present invention offers a number of advantages over the prior art. There is provided a digital video camera that has integrated intelligence.

Image data can at least be partially processed on board the current camera such as priority data (e.g. alarm or an unusual situation) is determined at the camera and stored and transmitted to the front end of the monitoring system.

Likewise, similar advantages are possible with a digital audio device such as an intercom.

The present invention also provides a monitoring system in which data can be processed at the surveillance camera which prevents "information overload" at the front end of the system.

As with the visual digital camera, the digital intercom can also process data in a similar way, for example with compression techniques, and event bracketing provided by having a buffer system that allows data to be stored before, during and after an event and so forth.

Communication of selected data reduces the information of the load that the conventional operators can be subject to. It also reduces the requirement for large band-width communication between the camera and the monitoring system.

BRIEF DESCRIPTION OF DRAWINGS

Aspects of the present invention will now be described by way of example only with reference to the accompanying drawings in which:

Figure 1 is a schematic diagram illustrating basic functional blocks of a digital video camera in accordance with one embodying present invention and,

Figure 2 is another schematic diagram indicating the workings of a digital video camera in accordance with one embodiment present invention and,

Figure 3 is a schematic view of memory allocation in accordance with one embodiment of the present invention and,

Figure 4 shows the transitions of the image states and functions that cause them in accordance with one embodiment of the present invention.

BEST MODES OF PRESENT INVENTION

Referring firstly to Figure 1 of the drawings the DVC consists of six basic functional blocks as shown. The communications block 10 is in the system being described herein the CARDAX™ Local BUS interface for the camera. As will be appreciated by those skilled in the art galvanic isolation can be provided between the camera electronics and the Local BUS communication lines which can also be provided with protective devices.

The communications block 10 is based around a microprocessor with various integrated peripherals including parallel and serial ports. The microprocessor is provided with FLASH E^2 PROM non-volatile memory to hold programme code and set-up data and volatile SRAM memory for general use.

The non volatile memory holds programme code and set-up data for both the communications block 10 and the main processing block 11. The communications block 10 down-loads main programme code and set-up data as required (for example, at power-up reset) to the main processing block 11 which is provided only with volatile memory for data and programme control. In normal operation programme code and set-up data can be updated/down-loaded from an external device via the Local BUS interface. Several different versions of programme code and set-up data for both the communications block 10 and the main processing block 11 may be stored in the non-volatile memory. Software control mechanisms select the version(s) to be used in any particular time.

The communications block 10 can also provide unit address initialisation, unique electronic serial number identification, tamper detection, micro-controller supervisory functions, and visual processing indications using LEDs.

The main processing block 11 is based around a digital signal processor ("dsp"). The dsp is provided with SRAM which it can flexibly segment into areas of data and programme code memory. The dsp primarily analyses images and compresses data.

A multi-functional "host port" associated with the dsp in processing block 11 connects to the address and data BUS system of the communications block 10 to